

What is claimed is:

1 1. A detection circuit for detecting whether a signal
2 is oscillating, comprising:
3 first detect circuitry, comprising:
4 at least one capacitive element;
5 a first circuit for placing, at a first drive
6 strength, a first voltage across the at least one
7 capacitive element; and
8 a second circuit for selectively placing, at a
9 second drive strength greater than the first drive
10 strength, a second voltage across the at least one
11 capacitive element when activated, the second circuit
12 being coupled to receive the signal and being activated
13 based upon a value of the signal; and
14 an output circuit having an input coupled to the
15 capacitive element and having an output having a value based
16 upon the voltage appearing across the capacitive element.

1 2. The detection circuit of claim 1, wherein the first
2 voltage is a voltage representative a first logic value and
3 the second voltage is a voltage representative of a second
4 logic value.

1 3. The detection circuit of claim 1, wherein the first
2 logic value is a logic high value and the second logic value
3 is a logic low value.

1 4. The detection circuit of claim 1, wherein the first
2 circuit comprises a current source for sourcing current to
3 the at least one capacitive element.

1 5. The detection circuit of claim 4, wherein the
2 current source comprises at least a portion of a current
3 mirror having a first current leg and a second current leg
4 coupled to the at least one capacitive element.

1 6. The detection circuit of claim 4, wherein the second
2 circuit comprises a transistor coupled across the at least
3 one capacitive element, a control terminal of the transistor
4 being coupled to the signal.

1 7. The detection circuit of claim 6, wherein the
2 transistor of the second circuit is sized larger than the
3 size of transistors in the second current leg of the current
4 mirror.

1 8. The detection circuit of claim 6, further comprising
2 a third circuit for initially placing the second voltage
3 across the at least one capacitive element when enabled.

1 9. The detection circuit of claim 1, wherein the second
2 circuit comprises a Schmitt-trigger circuit having an input
3 coupled to the at least one capacitive element and an output
4 coupled to an input of the output circuit.

1 10. The detection circuit of claim 1, further
2 comprising:
3 second detect circuitry, comprising:
4 at least one capacitive element;
5 a first circuit for placing, at a third drive
6 strength, one of the first and second voltages across
7 the at least one capacitive element of the second
8 detect circuitry; and
9 a second circuit for selectively placing, at a
10 fourth drive strength greater than the third drive
11 strength, the other of the first and second voltages
12 across the at least one capacitive element of the
13 second detect circuitry when activated, the second
14 circuit of the second detect circuitry being coupled to
15 receive the signal and being activated based upon a
16 value of the signal, the at least one capacitive
17 element of the second detect circuitry being coupled to
18 an input of the output circuit so that the output of
19 the output circuit is based in part upon a voltage
20 appearing across the at least one capacitive element of
21 the second detect circuitry.

1 11. The detection circuit of claim 10, wherein the
2 signal activates the second circuit of the first detect
3 circuitry when in a first logic state and activates the
4 second circuit of the second detect circuitry when in a
5 second logic state different from the first logic state.

1 12. The detection circuit of claim 10, further
2 comprising circuitry for initially placing the first voltage
3 across both of the at least one capacitive elements when
4 activated.

1 13. The detection circuit of claim 10, wherein the
2 first drive strength is substantially the same as the third
3 drive strength, and the second drive strength is
4 substantially the same as the fourth drive strength.

1 14. A method for detecting whether a signal is
2 oscillating between at least two logic states, comprising:
3 initially placing a first voltage level across at least
4 one first capacitive element;
5 driving, with a first drive strength, a voltage
6 appearing across the at least one first capacitive element
7 towards a second voltage level;
8 selectively driving, with a second drive strength
9 greater than the first drive strength, the voltage across the
10 at least one first capacitive element towards the first
11 voltage level when the signal is in a first of the at least
12 two logic states; and
13 generating an output signal having a value based upon
14 a voltage level across the at least one first capacitive
15 element.

1 15. The method of claim 14, wherein the first voltage
2 level corresponds to a logic low value and the second voltage
3 level corresponds to a logic high value.

1 16. The method of claim 14, wherein the second voltage
2 level corresponds to a logic low value and the first voltage
3 level corresponds to a logic high value.

1 17. The method of claim 14, wherein the output signal
2 switches between first and second logic states based upon the
3 voltage appearing across the at least one first capacitive
4 element relative to a predetermined voltage between the first
5 voltage level and the second voltage level.

1 18. The method of claim 14, further comprising:
2 initially placing a third voltage level across at least
3 one second capacitive element;
4 driving, with a third drive strength, a voltage
5 appearing across the at least one second capacitive element
6 towards a fourth voltage level;
7 selectively driving, with a fourth drive strength
8 greater than the third drive strength, the voltage across the
9 at least one second capacitive element towards the third
10 voltage level when the signal is in a second of the at least
11 two logic states, wherein the output signal has a value based
12 upon a voltage level across the at least one second
13 capacitive element.

1 19. The method of claim 18, wherein the first voltage
2 level is approximately equal to the third voltage level and
3 the second voltage level is approximately equal to the fourth
4 voltage level.

1 20. The method of claim 18, wherein the first voltage
2 level is approximately equal to the fourth voltage level and
3 the second voltage level is approximately equal to the third
4 voltage level.

1 21. The method of claim 18, wherein the third drive
2 strength is substantially the same as the first drive
3 strength, and the fourth drive strength is substantially the
4 same as the second drive strength.

1 22. An apparatus, comprising:
2 a first circuit that generates an output signal; and
3 a second circuit having an input coupled to the output
4 signal of the first circuit, the second circuit detecting
5 whether the output signal of the first circuit oscillates at
6 a frequency that is less than a predetermined frequency, the
7 second circuit capable of determining whether the output
8 signal of the first circuit remains in a first logic state
9 for at least a predetermined period of time and in a second
10 logic state for at least the predetermined period of time.

1 23. The apparatus of claim 22, wherein the second
2 circuit comprises:

3 a first capacitive element;

4 a third circuit for charging the first capacitive
5 element towards a first voltage level;

6 a fourth circuit for selectively charging the first
7 capacitive element towards a second voltage level at a drive
8 strength greater than a drive strength at which the third
9 circuit charges the first capacitive element, the fourth
10 circuit being activated when the output signal of the first
11 circuit is in the first logic state; and

12 a fifth circuit having an input coupled to the first
13 capacitive element for generating an output signal having a
14 value dependent upon the voltage appearing across the first
15 capacitive element.

1 24. The apparatus of claim 23, wherein the first
2 voltage level corresponds to a logic low state and the second
3 voltage level corresponds to a logic high state.

1 25. The apparatus of claim 23, wherein the first
2 voltage level corresponds to a logic high state and the
3 second voltage level corresponds to a logic low state.

1 26. The apparatus of claim 23, further comprising:
2 a second capacitive element;
3 a sixth circuit for charging the second capacitive
4 element towards a third voltage level;
5 a seventh circuit for selectively charging the second
6 capacitive element towards a fourth voltage level at a drive
7 strength greater than a drive strength at which the sixth
8 circuit charges the second capacitive element, the seventh
9 circuit being activated when the output signal of the first
10 circuit is in the second logic state, the value of the output
11 signal of the fifth circuit being based upon the voltage
12 level appearing across the second capacitive element.

1 27. The apparatus of claim 26, wherein the first
2 voltage level is substantially the same as the third voltage
3 level and the second voltage level is substantially the same
4 as the fourth voltage level.

1 28. The apparatus of claim 26, wherein the first
2 voltage level is substantially the same as the fourth voltage
3 level and the second voltage level is substantially the same
4 as the third voltage level.

1 29. The apparatus of claim 26, wherein the sixth
2 circuit comprises at least a portion of a current mirror.

1 30. The apparatus of claim 23, wherein the third
2 circuit comprises at least a portion of a current mirror.

1 31. The apparatus of claim 23, wherein the first
2 voltage level corresponds to a logic high state and the
3 second voltage level corresponds to a logic low state.